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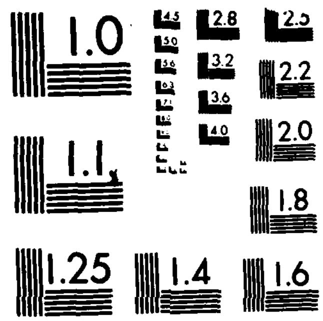

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AD-A142 252

EIGHTH EUROPEAN SPECIALIST WORKSHOP ON
'ACTIVE MICROWAVE SEMICONDUCTOR DEVICES'

4 - 6 MAY 1983

PROGRAMME
AND
BOOK OF ABSTRACTS

DAJA45-83-M-0168

CREST HOTEL, MAIDENHEAD, BERKS., UK

Workshop Coordinators

Professor P N Robson	)	Sheffield University, UK
Dr J E Sitch	)	

Advisors

Austria:	Professor H Thim
France:	Dr J Magarshack
	Dr D Pavlidis
Germany:	Professor H L Hartnagel
	Professor E Hesse
Italy:	Professor V Svelto
Japan:	Dr S Kataoka
Sweden:	Professor P Weissglas
UK:	Dr K W Gray
USSR:	Dr D P Tsarapkin
USA:	Professor L F Eastman

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Eighth European Specialist Workshop on
'Active Microwave Semiconductor Devices'
Crest Hotel, Maidenhead, UK: 4 - 6 May 1983

Programme

Wednesday 4 May 1983

08.30 hrs	Introduction
	MATERIALS PREPARATION AND DEVICE PROCESSING
08.45 hrs	'OMVPE applied to the growth of active microwave devices' S D Hersee, J P Hirtz, M Razeghi, J P Duchemin, J L Pinsard Thomson-CSF, France
09.15 hrs	'Resistivity and mobility distribution in bulk LEC undoped semi-insulating GaAs wafers for IC applications' N Visentin, M Bonnet, B Gouteraux, B Lent Thomson-CSF, France
09.30 hrs	'The implant dose and anneal temperature dependence of the redistribution of Mg implants in GaAs' R Sweda, R T Blunt Plessey Research (Caswell) Ltd, UK
09.45 hrs	'Si implantation into LEC undoped high resistivity GaAs for IC applications' E Kohn, T Pham Phan, J Icole, M Cathelin, A Huber Thomson-CSF, France
10.00 hrs	'Characterisation of semi-insulating GaAs by the temperature-dependent hall effect' G Pacheiser Siemens AG, Federal Republic of Germany
10.15 hrs	'Si impatt material grown by low pressure VPE' T B F Joyce, J E Curran, A Hing, J L B Walker GEC Hirst Research Centre, UK
10.30 hrs	'Fabrication induced damage during dry processing of GaAs integrated circuits' D A Allan, P J Smith British Telecom Research Laboratories, UK
10.45 hrs	'Influence of contact properties and dopant concentration on quasi-two-dimensional electron gas field effect transistor characteristics' H Damkes, K Heime Universitat Duisberg, Federal Republic of Germany E Schubert, K Ploog Max-Planck-Institut, Federal Republic of Germany G Weimann DBP, Federal Republic of Germany
11.00 hrs	COFFEE

11.15 hrs	'Influence of the surface conditions on the characteristics of self aligned GaAs MESFETs' A Cetronio, R Graffitti, S Moretti, M Bujatti* Selenia Research Laboratories, Italy *currently with Hewlett Packard Technology Centre, USA
	FET DEVICES
11.30 hrs	'Microwave applications of high electron mobility transistors' T Misugi, M Abe, T Mimura, H Komizo Fujitsu Laboraories Ltd, Japan
12.00 hrs	'Microwave performance of two-dimensional electron gas FETs' N T Linh Thomson-CSF, France
12.30 hrs	LUNCH
	FET DEVICES (contd)
14.00 hrs	'Selectively-doped heterojunction transistors and circuit developments at Bell Laboratories' R Dingle Bell Labs, USA
14.30 hrs	'Average and differential mobility measurements in submicron-gate modulation doped $Al_xG_{1-x}As/GaAs$ heterojunction FETs' R H Wallis, P Delescluse, M Laviron, D Delagebeaudeuf Thomson-CSF, France
14.45 hrs	'Monte-Carlo 2-dimensional MESFET simulation' M A R Al-Mudares, K W H Foulds University of Surrey, UK
15.00 hrs	'Stabilised fin-line FET oscillators' A Jacob, C Ansorge, K Schünemann Technische Universitat Braunschweig, Federal Republic of Germany
15.15 hrs	'Broad-band, medium power electronically tunable oscillators' M J Howes University of Leeds, UK
15.30 hrs	'High gain 20GHz power FETs: design optimization and performance' P M White, B Liles, A Peake, B S Hewitt Raytheon Co, USA
15.45 hrs	'An improved dual-gate MESFET frequency doubler' H V Shurmer University of Warwick, UK
16.00 hrs	TEA

09.30 hrs	'*Bipolar* heterojunction transistors for high performance linear and ultra high speed digital circuits - an investigation of the potential' G W Sumerling, R Goodfellow, I Griffiths, C Wilkins Plessey Research (Caswell) Ltd, UK
09.45 hrs	'Edge crowding phenomenon analysis in GaAlAs-GaAs hetrojunction bipolar microwave transistors' Y Druelle, Y Crosnier, G Salmer University of Lille, France
	<u>GaAs ICs</u>
10.00 hrs	'Monolithic integrated circuit mixers for the millimetre and sub-millimetre wave regions' B Clifton Lincoln Labs, USA
10.30 hrs	'The performance of GaAs MMIC lumped element phase shifter at S and C band' C W Suckling, P N Rigby, T B Bambridge R S Pengelly, R S Butlin Plessey Research (Caswell) Ltd, UK
10.45 hrs	'A two-stage, modular cell monolithic power amplifier' D Pavlidis, J Magarshack Thomson-CSF, France
11.00 hrs	COFFEE
11.15 hrs	'The noise figure of the microwave distributed amplifier using FETs' C S Aitchison Chelsea College, UK
11.30 hrs	'MIM capacitor dielectrics for GaAs MMICs' P R Jay, J Pichon Thomson-CSF, France T Girma University of Bordeaux, France
11.45 hrs	'A broadband planar GaAs amplifier/oscillator for monolithic micro and millimeter wave ICs' R Kuch, K Lubke, G Rieder, R Charicovsky, H Thim Technical University of Vienna, Austria
12.00 hrs	'1.12 Gb/s multiplexer IC on GaAs for laser modulation' K Mause DBP, Federal Republic of Germany
12.15 hrs	'GaAs clocked comparator operating at 1.8GHz' D Meignant, M Binet LEP, France
12.30 hrs	LUNCH
14.30 - 17.30 hrs	Boat Trip on the Thames
20.00 hrs	Banquet in Shoppenhanger's Manor

16.15 hrs 'Self aligned ion-implanted T-gate technology for high-speed GaAs logic'
R A Sadler, L F Eastman
Cornell University, USA

16.30 hrs 'Effects of cooling on a GaAs MESFET's logic circuit - computed and experimental results'
M Henry, J Kamden, J P Klein, M Le Rouzic, P Urien
CNET Lannion, France

16.45 hrs 'Electron-beam fabricated sub-micron gate GaAs FETs for microwave and logic circuits'
L H Camnitz, W L Jones, H Lee, L F Eastman
Cornell University, USA

17.00 hrs 'Computer modelling of a dual gate MESFET mixer'
R E Miles
University of Leeds, UK

17.15 hrs 'Two-dimensional simulation of submicronic space charge modulated FET structures'
R Fauquembergue, M Pernisek, E Constant
University of Lille, France

17.30 hrs 'A computer simulation of small signal compression on GaAs FET limiting amplifier'
L Raffaelli
Elettronica SpA, Italy

17.45 hrs 'A physical model for the large-signal characterisation of microwave MESFET operation'
C M Snowden
University of York, UK

18.00 hrs 'Comparative survey of several models for submicrometer gate FETs'
G Salmer, S E I Ghazali, M Lefebvre, E Constant
University of Lille, France
M Ibrahim
Cairo University, Egypt

Thursday 5 May

BIPOLAR DEVICES

08.45 hrs 'GaAs heterojunction bipolar transistors for microwave applications'
D Ankri
CNET, France

09.15 hrs 'Design and fabrication of GaAlAs/GaAs bipolar transistors: application to power microwave devices'
G Rey, J P Bailbe, A Marty
CNRS, France

Friday 6 May

NOVEL DEVICES, MATERIALS AND EFFECTS

09.00 hrs	'$Ga_{0.47}In_{0.53}As$ FETs and related problems' H Beneking Technical University, Aachen, Federal Republic of Germany
09.30 hrs	'High velocity electrons for compound semiconductor transistors' L F Eastman Cornell University, USA
10.00 hrs	'The properties and performance of monolithic hot electron transistors' J M Shannon Philips Research Laboratories, UK
10.30 hrs	'InP/InGaAsP bipolar transistors for optical receivers' D Fritzsche, H Birkhard, E Kuphal DBP, Federal Republic of Germany
10.45 hrs	'High power InP MISFETs' M Armand, D V Bin, J Chevrier, N T Linh Thomson-CSF, France
11.00 hrs	COFFEE
11.15 hrs	'The pulse behaviour of quasi normally-off GaAs MISFETs' G Swanson Chelsea College, UK

TWO TERMINAL DEVICES

11.30 hrs	'Improved noise performance of millimetre wave silicon Impatts' M R B Jones, D M Brookbanks Plessey Research (Caswell) Ltd, UK
11.45 hrs	'On the efficiency of pulsed and CW Impatt diodes' J L B Walker GEC Hirst Research Centre, UK
12.00 hrs	'Fast risetime GaAs read Impatts' B J Buck and D M Brookbanks Plessey Research (Caswell) Ltd, UK
12.15 hrs	'Electronic tuning of Trapatt oscillators' N Nazoa-Ruiz, C Aitchison Chelsea College, UK

Post-Deadline Papers

12.30 hrs	'Interface formation of metal on MBE-grown GaAs (001)' T G Andersson, S P Svensson, J Kanski, G Landren Chalmers University of Technology, Sweden
	LUNCH

OMVPE Applied to the Growth of Active Microwave Devices

S.D. Hersee, J.P. Hirtz, M. Razeghi, J.P. Duchemin and J.L. Pinsard

Th ·mson-CSF, Domaine de Corbeville, 91401 Orsay Cedex, France

We are investigating the use of OMVPE at low pressure to grow several types of active microwave device, including : GaAs MESFETs, InP Gunn diodes and GaAs/GaAlAs modulation doped heterojunctions (for "TEGFET" applications).

In this presentation we will describe the growth technique and show how the use of a laminar gas flow and a "diffusion-controlled" growth regime gives advantages in the control of epi-layer uniformity and in the growth of the very abrupt heterojunctions that are required for the modulation doped structures.

GaAs MESFETs have now been grown in the small (substrate area $\leq 10\ cm^2$) and large scale MR 200 reactor. The DC characteristics of unbuffered devices show "looping" which is probably related to the accumulation of Cr and Fe at the substrate/epitaxy interface as identified by SIMS. MESFETs with a buffer show no looping and exhibit typical transductance values that are equivalent to $AsCl_3$ grown structures. Pinch off voltages are still higher than required due to the current leakage into the buffer layer.

The study of a 3 layer InP Gunn diode structure is still at an early stage but it would appear that growth at 550°C gives sharp n^+/n^- doping changes and that there is a lower defect density in the OMVPE grown material than in conventionally grown (PCl_3)InP.

GaAs/GaAlAs modulation doped heterostructures have been grown by OMVPE with mobilities at 4 K of up to 162,000 $cm^2V^{-1}s^{-1}$. The sheet carrier concentration in the 2 DEG was controlled by the width of the undoped spacer layer and at low concentrations there was evidence of trapping in the GaAlAs. Each of these three applications will be discussed in detail showing the advantages and sometimes disadvantages of OMVPE by comparison with more conventional growth techniques.

Resistivity and Mobility Distribution in Bulk LEC Undoped Semi-Insulating GaAs Wafers for IC Applications

N. Visentin, M. Bonnet, B. Gouteraux and B. Lent

Thomson-CSF/LCR domaine de Corbeville, 91401, Orsay, France.

A complete study of the influence of the semi-insulating substrate on an implanted layer and consequently on the circuits has involved the setting up of an automatic system for measuring the electrical properties of the material (resistivity Hall constant, Hall mobility). The spreading of properties over a wafer is obtained by drawing bar charts of the data (mean value standard deviation) and the homogeneity patterns are plotted in the form of colour coded maps (800 measurements on a 2 inch wafer).

A systematic analysis made on undoped boules pulled in a P-BN crucible has shown :

- A radial and longitudinal dispersion of the electrical properties :

  $\bar{\rho}_{400K} \pm \Delta\rho = 4.8\ 10^{4} \pm 0.7\ 10^{4}\ \Omega.cm$ to $7.6\ 10^{4} \pm 1.4\ 10^{4}\Omega.cm$

  $\bar{R}_{H400K} \pm \Delta R_{H} = 1.5\ 10^{8} \pm 0.2\ 10^{8} Cb^{-1}.cm^{3}$ to

  $2.6\ 10^{8} \pm 0.4\ 10^{8}\ Cb^{-1}.cm^{3}$

- A variation in the homogeneity pattern presenting either a quadratic symmetry or a revolution symmetry.

- Regions of better homogeneity in the ingot.

Using the same method we have analyzed and compared materials from several available sources.

The Implant Dose and Anneal Temperature Dependence of the Redistribution of Mg Implants in GaAs.

R. Sweda, R.T. Blunt

Plessey Research (Caswell) Ltd., Allen Clark Research Centre, Caswell, Towcester, Northants.

Of major importance to the future of bipolar devices based on GaAs is the development of a viable acceptor implant technology. To fulfil the need for a suitable implant species, magnesium has much to commend it, and yet we have found that during implant activation anneal the Mg^+ suffers significant redistribution. To investigate the limits of this behavious, wafers of undoped S.I. GaAs were given implant doses of 10^{13} or 10^{14} ions cm^{-2} at 100keV. After encapsulation with reactively sputtered silicon nitride the wafers were annealed at either 750°C or 850°C. Carrier concentration and mobility profiles of the annealed samples were obtained by differential Hall profiling using anodic oxidation and stripping whilst atomic profiles were obtained using S.I.M.S. Without exception, the shapes of electrical and atomic profiles showed close similarity and whereas it was absent at the lower doses, a marked redistribution of magnesium occurred at the higher doses. Moreover, S.I.M.S. atomic profiles through the nitride cap revealed that the magnesium redistribution apparently extended into the cap itself; up to 250A from the GaAs-Si_3N_4 interface. Results will be presented to demonstrate that the magnesium redistribution is both ion dose and anneal temperature dependent and can result in, at worst, 25% of the implant dose being lost into the cap.

Si Implantation into LEC Undoped High Resistivity GaAs for IC Applications

E. Kohn, T. Pham Phan, J. Icole, M. Cathelin, A. Huber**

Thomson - C.S.F. - D.C.M./D.A G. - B.P. No.10 - 91401 Orsay, (France)
**Thomson - C.S.F. - L.C.R. - B.P. No.10 - 91401 Orsay, (France)

Si implantation into LEC - undoped substrates of high resistivity(*) has been optimized for a variety of applications in digital and μW integrate circuit technology.

Firstly, different annealing techniques (i.e. capless annealing and annealing under a Si_3N_4 cap) are compared to achieve reproducibly an activation above 90%. The highest reproducibility was found for a process which includes implantation through a sputtered Si_3N_4 film which also serves as the annealing cap. The optimization of the implantation procedure will be described. This includes experiments with a fast annealing technique and the variation in the capping parameters. Special emphasis is placed on the characterization of the GaAs near surface region by SIMS - analysis and ellipsometric measurements. Under optimum conditions the disturbed surface region is below 400Å.

Secondly, results of electrical doping and mobility profiles will be presented for a wide range of implantation parameters covering an implantation depth between 0.04μm and 0.4μm and doping levels between 8×10^{16} and $10^{18} cm^{-3}$. A typical value for the mobility at a doping level of $2 \times 10^{17} cm^{-3}$ is above 4000 cm^2/v.s. which compares well with epitaxial material, an activation above 90%, a compensating dose below $4 \times 10^{11}/cm^2$ and a homogeneity better than 5% in the pinch-off voltage and sheet resistance over a 2" wafer.

(*) The material properties are described in the paper of N. Visentin et al entitled : "Resistivity and Mobility Distribution in Bulk LEC-Undoped Si GaAs wafers for IC - Applications" also submitted to this workshop.

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Characterization of Semi-Insulating GaAs by the Temperature-Dependent Hall Effect

Dr. G. Packeiser

Siemens AG, Munich, Germany

Measurement of the temperature-dependent Hall effect has been used as a characterizing tool for different semi-insulating LEC materials including Chromium-doped GaAs and undoped material pulled from quartz and PBN crucibles. Experimental results are discussed in terms of the compensation models by R. Zucca and by G.M. Martin et al.

In most publications, Hall mobility has been taken constant in the whole temperature range. It turns out, however, that it is frequently necessary to take account of its temperature dependence - represented by an 'activation energy' E_μ. It is substantial in materials which are characterized by more than one conduction mechanism, e.g. Cr-free and highly Cr-doped GaAs pulled "in situ" from quartz crucibles. Especially in the first case this leads to a better understanding of its relatively unstable Hall properties indicating that a second deep donor at E_c-0.39eV is involved in the electrical compensation.

A comparison of the data of various LEC-materials shows that it is possible to distinguish between seven types of materials from a Hall experiment with temperature variation alone. Materials can thus be classified by means of six physical parameters : resistivity, carrier density, mobility, position of the dominant deep level, E_μ, and the type of conduction.

Si Impatt Material Grown By Low-Pressure VPE

T.B.F. Joyce, J.E. Curran, A. Hing and J.L.B. Walker

GEC Research Laboratories, Hirst Research Centre, Wembley, U.K.

Si Impatt for use at 100GHz require drift lengths of 0.3µm, but conventional atmospheric pressure reactors operating at 1050°C cause substantial degradation of the ideal flat - profile abrupt - interface structure for such thin epilayers. This paper will report on the use of low-pressure epitaxy at reduced temperature to overcome this limitation. This is believed to be the first reported use of low-pressure low-temperature epitaxy for Impatt diodes. Using this technique the interface abruptness between the substrate and epilayer has been improved from 0.15µm/decade at 1050°C to 0.05µm/decade at 900°C.

It will also be shown that in double drift structures the PN transition region can be modelled analytically by

$$N(x) = N_D \tanh \frac{x}{d}$$

where x = 0 represents the junction and N_D is the doping level far removed from the junction. For atmospheric pressure layers d ≈0.3µm. Using this expression it will be shown that this raises the breakdown voltage e.g. an ideal abrupt symmetrical double drift diode i.e. d = 0 with $N_D = N_A = 2 \times 10^{17} cm^{-3}$ has V_B = 11.5V but for d = 0.3µm V_B = 19V. This decreases the device efficiency. Furthermore, it will also be shown that the graded interface results in a more extended avalanche zone which further reduces efficiency.

Fabrication Induced Damage During Dry Processing of GaAs Integrated Circuits

D.A. Allan, P.J. Smith

British Telecom Research Laboratories, Ipswich, IP5 7RE.

The fabrication technology of GaAs integrated circuits based on MESFETs involves plasma and ion beam processes for semiconductor doping, dielectric deposition, pattern definition and metallisation. These processes subject the GaAs surface to a flux of energetic particles which can influence the electrical characteristics of the interface between the semiconductor and the Schottky diode forming the gate of the MESFET. In order to investigate damage induced by these processes, isolated steps in a typical fabrication sequence have been simulated on n-type GaAs layers, and the effects assessed by analysis of the I-V and C-V characteristics of Schottky diodes evaporated onto the treated surfaces. Deep Level Transient Spectroscopy has also been used to look for trapping levels introduced by the processing. The reduction and annealing of the induced damage within the constraints imposed by the processing technology have also been investigated.

The results of these investigations indicate that while many of these processes do introduce damage which degrades the Schottky diode characteristics, in most cases the damage can be annealed out at temperatures of 300°C or below thus making these processes compatible with the device fabrication. The effects of the damage can however influence device characteristics which can change during subsequent processing stages as the defects migrate or anneal out.

Influence of Contact Properties and Dopant Concentrations on Quasi-Two-Dimensional Electron Gas Field-Effect Transistor Characteristics

H. Dämbkes, K. Heime — Universität Duisburg

E. Schubert, K. Ploog — Max-Planck-Institut, Stuttgart

G. Weimann — Forschungsinstitut, DBP, Darmstadt

The existence of a quasi-two-dimensional electron gas (2DEG) in pure, undoped GaAs near an $Al_xGa_{1-x}As$/GaAs hetero interface ($x < 0.3$) has recently attracted considerable interest because of both the new physical phenomena (quantized HALL-effect) and the application to high-speed field-effect transistors (modulation-doped FET, MODFET; two-dimensional electron gas FET, TEGFET; high-electron mobility FET, HEMT).

In this paper experiments on TEGFETs with 1μm gate length made from differently composed heterostructures are described, which are focussed on the influence of contact properties and sheet resistivities of the 2 DEG on device behaviour, especially on transconductance g_m and on-resistance R_{on}.

By using a test cell with several FETs having different source-drain spacings and from a transmission-line structure the contributions of both *ohmic contact resistivity* and the 2 DEG-sheet resistivity could be separated. Good ohmic contacts are difficult to make because the 2 DEG is very thin (extremely small contact area) and the 2 DEG is destroyed under the alloyed contact region. High contact resistances decrease g_m, increase R_{on} and sometimes result in blocking characteristics at low temperatures (<77K). By a careful control of the alloy process we succeeded in obtaining contact resistances of 0.2Ωmm. The remaining relatively high values of R_{on} in the FETs are shown to be determined by the sheet resistivity of the 2 DEG. As long as the thickness of AlGaAs is limited to about 50nm at the maximum achievable donor concentration of $\approx 10^{18}cm^{-3}$ in order to avoid a parallel conductance in the AlGaAs the sheet resistivity is limited to 1,2KΩ per square (assuming that 10% of the electrons are transferred into the 2 DEG). This is inferior to "normal" GaAs MESFETs, where a sheet resistivity of less than 100Ω per square is obtained using the recessed gate technology. Hence g_m (300K) of TEGFETs is lower than that of good GaAs MESFETs. A "recessed-gate like" structure should overcome these disadvantages by deliberately introducing a parallel conductance in the AlGaAs and/or in an additional n^+-GaAs layer on top of the AlGaAs outside the gate-region. Only then full advantage of the high electron mobility will be taken at room temperature.

This work is supported in part by "Stiftung Volkswagenwerk"

Influence of the Surface Conditions on the Characteristics of Self-Aligned GaAs MESFETs

A. Cetronio, R. Graffitti, S. Moretti, M. Bujatti*

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The transconductance of GaAs MESFETs can be appreciably affected by the surface treatment of the channel region, an effect which is also found to be strongly dependent on the type of passivation used.

In this paper we shall demonstrate that for self-aligned Al-gate MESFET's this phenomenon is not due to the accumulation of arsenic at the Al-GaAs interface as suggested by Singh et al(1) but most probably due to the formation of small traces of H_2O_2 in the phosphoric-acid based aluminium etchant.

Furthermore by passivating our devices with different insulating films, such as SiO, Si_3N_4 and polyimide and by comparing these with unpassivated devices (all on the same wafer) it appears that the insulating films *strongly influence* the device transconductance only if the active layer surface conditions are imperfect, as suggested by Ozeki et al(2).

References

1) B.R. Singh, O.P. Daga, M. Kochhar, W.S. Khokle, Solid State Electronics, 25(12) , 1209 (1982).

2) M. Ozeki, K. Kodama, and A. Shibatomi, Fujitsu Sci Tech.J., 18(4), 475 (1982).

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Microwave Application of High Electron Mobility Transistors

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The High-Electron Mobility Transistor (HEMT) is a new device utilizing a modulation-doped GaAs-GaAlAs heterojunction structure and is expected to provide high performance of LSI for high speed computers. They have a switching propagation delay time of 16.8ps at room temperature and 12.8ps at 77K, which is the highest speed compared with any kind of transistors.

These high performances in digital applications suggest that HEMT will provide a lower noise figure and a higher gain than the conventional Si and GaAs FETs in analog application such as that of microwaves.

The performance was obtained in discrete microwave HEMT with 0.5μm gate length. At 12GHz a noise figure of 1.4dB and associated gain of 11dB were obtained at room temperature. The measured cut-off frequency was 30GHz at a bias condition of I_{ds} = 10mA. A lower ambient temperature, 100K, noise figure of 0.35dB and associated gain of 12.5dB were measured.

Microwave Performance of Two-Dimensional Electron GaAs FETs

Nuyen T. Linh

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Since the first realizations of two-dimensional electron gas FETs (TEGFETs) for low noise amplification and high speed logic, questions are still opened on their real capabilities. This paper will present new results on low noise and high speed TEGFETs which confirm their intrinsic superiority over conventional GaAs FETs.

0.5 - 0.6μm gate length TEGFETs present a noise figure of 1.3dB and an associated gain of 11dB at 10GHz, in spite of a high value of the source resistance (2.3Ω/mm). By applying the Fukui equation :

$$F = 1 + 2\pi C_{gs} f K \sqrt{R_s + R_g / g_{mo}},$$

the K factor has been found to be 1.5, which is much lower than the value of 2.5 observed on the best GaAs FETs. The decrease of noise figure with temperature is stronger on TEGFET than GaAs FET. Results on one quarter micron transistors will be given.

High speed logic circuits with propagation delay times of less than 18ps will also be presented.

Finally, experimental results will be discussed in terms of electron velocity enhancement, overshoot effect, two-dimensionality and parasitic series resistances.

Average and Differential Mobility Measurements in Submicron-Gate Modulation Doped $Al_xGa_{1-x}As/GaAs$ Heterojunction FETs

R.H. Wallis, P. Delescluse, M. Laviron and D. Delagebeaudeuf

Laboratoire Central de Recherches, Thomson-CSF, B.P. No.10, 91401 Orsay (France)

In modulation-doped $Al_xGa_{1-x}As/GaAs$ structures, enhanced mobilities are achieved by spatially separating the electrons from their parent donors on opposite sides of the heterojunction. However high values will result only if complete electron transfer from the hightly-doped and low mobility $Al_xGa_{1-x}As$ layer to the potential well on the GaAs side of the heterojunction is achieved. At low temperatures, where spectacularly high mobiiities have been reported, any carriers remaining in the $Al_xGa_{1-x}As$ are frozen out : for room temperature device applications their contribution cannot be ignored.

We report here room temperature measurements in gated structures in which the gate bias has been used to investigate the variation of mobility with total electron density. Our measurements have been taken on real (i.e. submicron gate) devices rather than test structures, and are thus directly applicable to device modelling. Our experimental method recognizes that the high width-to-length ratio of a typical FET means that the average mobility of all electrons μ_{av} may be determined directly from the geometric magnetoresistance of the channel, and that furthermore, by modulating the gate bias V_g and determining the magnetotransconductance, the differential mobility μ_{diff} (i.e. the mobility of the modulated electrons) may also be obtained.

Our results show, as a function of increasingly negative gate bias, three regimes : (i) for V_g near zero, μ_{av} is large, since the high mobility electrons at the interface dominate, but μ_{diff} is very small, since the $Al_xGa_{1-x}As$ is not fully depleted and it is primarily its population which is modulated; (ii) for V_g more negative, the $Al_xGa_{1-x}As$ becomes fully depleted, and both μ_{av} and μ_{diff} are large (greater than in bulk GaAs of equivalent electron concentration); (iii) finally, as V_g approaches pinch-off, both μ_{av} and μ_{diff} fall (typically by a factor of two), showing that the enhanced mobility is not only a consequence of reducing ionized impurity scattering but that the enhanced screening produced by the locally high electron density at the interface also plays a role.

Monte Carlo 2-dimensional MESFET Simulation

M.A.R. Al-Mudares and K.W.H. Foulds

Dept. of Physics, University of Surrey, Guildford, Surrey GU2 5XH. U.K.

The paper will present for the first time detailed results derived from a Monte Carlo two-dimensional simulation of practical FET structures including the substrate. It will discuss primarily the physical interpretation of the computer results and will deal with three areas of interest :

1. Factors which determine the existence of current drop back in the I-V characteristic,
2. velocity overshoot,
3. the effective mobility in heterostructure FETs.

Sections 1 and 2 will be dealt with rather briefly since it is felt that section 3 is most important at this time.

Brief details are as follows :

1. We shall comment particularly on the role that the transverse electric field plays in determining the relation between the longitudinal velocity and the longitudinal electric field and how this determines the form of the I-V characteristic.
2. The presence of velocity overshoot associated with short gates depends as much upon the increased gradient of the longitudinal electric field at the source-gate transition as upon the reduced transit time.
3. It is shown that a MESFET based on the heterostructure (undoped) GaAs/AlGaAs (n-type $10^{17}cm^{-3}$) does not necessarily lead to the same high mobility which might be expected from Hall effect measurements made on such heterostructures. For thin GaAs layers ($\approx$ 0.2um) the electrons under the gate are driven back into the doped AlGaAs with its relatively low mobility. The paper will discuss various structures which do lead to higher effective mobility.

Stabilized Fin-Line FET-Oscillators

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The increasing interest in FET circuits up to mm-waves has led us to the development of fin-line FET-oscillators through X- and Ku-Band up to Ka-Band. The stabilization problems of fin-line circuits (poor quality-factor and bad thermal characteristics) was solved by using dielectric resonators (DR) which were appropriately coupled to the fin-line. Two concepts have been pursued: fundamental wave oscillators for the frequency range up to 20GHz and second harmonic oscillators stabilized at their fundamental frequency for Ka-Band.

For ease of handling we have carried out all our experiments with packaged FETs, thus achieving a better flexibility at the expense of performance. The FET was soldered in a cross of 2 fin-lines. Three of the slots match the FET by means of sliding shorts while the fourth at the drain of the FET is connected to the waveguide output by means of an exponential taper. Feedback is performed by means of a metal strip connected on the back side of the circuit between drain and gate. The slot width has to be properly adjusted. These parameters are sufficient to fix output frequency and maximize output power.

As an example we got 15dBm at 11GHz (η = 38%). The pushing figure of $\Delta f_o/\Delta V_{DS}$ = -30MHz/V could be reduced by two orders of maghitude by introducing a DR mounted as a reaction cavity. At 20GHz an efficiency of 15% has been obtained at the fundamental frequency. Finally the unstabilized second harmonic oscillator yielded 7% efficiency at 31.4GHz. Stabilization at its fundamental frequency gave a pushing figure of 6MHz/V at the expense of 0.4 dB of output power.

Broad-Band, Medium-Power Electronically Tunable Oscillators

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The problem of realising MESFET microwave oscillators based on reasonably accurate design techniques has been tackled by a number of workers in recent years. However, whilst the main effort has been focussed on broad-band designs, high-power single-frequency designs or even low noise configurations, the possibility of developing a design procedure for broad-band electronically tunable MESFET oscillators which deliver maximum output power over the band has received little attention.

In the present work a logical approach to the design of varactor tuned oscillators based on MESFETs, which takes into account the inevitable restrictions due to practical device structures, is described. The design technique is such that the output power is maximised over the band. Full account has been taken of the nonlinear behaviour of the frequency tuning element. A suspended substrate realisation of a frequency agile oscillator based on this theory will be discussed. This oscillator is characterised by a tuning bandwidth of 4.5GHz at a centre frequency of ~10GHz and a maximum output power of 250mW.

High Gain 20 GHz Power FETs : Design, Optimization and Performance

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High performance K-band FETs are increasingly in demand for various microwave systems. Although a power capability to 1 W at 20 GHz has been demonstrated, the associated gains reported have been relatively low [1-3]. In this paper we describe devices which have achieved a linear gain of 8 dB at 20 GHz with an associated 1 dB compressed power output of 28 dBm and saturated power output of 29.5 dBm. The devices were 1.6 mm total gate width via-hole chips, similar to ones described previously [1], mounted on a miniature carrier suitable for insertion into microstrip circuitry. The high associated gains are attributed to a proper optimization of sub-micron gate length and active layer carrier concentration. Optimization was accomplished empirically using a special technique to systematically reduce the gate length on completed devices, thus facilitating a direct study of its effect on gain, power and efficiency. Results are presented for devices of differing active carrier concentration.

The limitations of current device structures at K-band frequencies are discussed and a novel design approach is proposed aimed at overcoming one of the serious parasitic problems. Preliminary performance data is presented for 1W, 20 GHz and 2W, 20 GHz devices using this unique design approach.

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An Improved Dual-Gate MESFET Frequency Doubler

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A dual-gate GaAs MESFET has been used in a novel manner to obtain improved frequency doubling at 6.8GHz output. Two basic forms of non-linearity are available in FET harmonic generators. One of these is the gate voltage/gate current non-linearity and the other is the gate voltage/drain current input non-linearity. Use of the former, however, requires that gate current is permitted to flow, but with a MESFET this has a deleterious effect upon the Schottky barrier associated with the gate. In the present work, therefore, the exponential region of the transfer characteristics of a dual-gate device has been used.

Examination of the effects of phase shift upon the efficiency of harmonic generation suggested that the provision of quadrature-related signals at the two gates would enhance the efficiency. In order to test this idea, a phase-splitting network was introduced so as to provide inputs to the two gates which were in phase quadrature. With such an arrangement, results were obtained which compared very favourably with previous reports, the best performance being obtained at an input signal level of about -10dBm. Further improvements are to be expected through optimisation of the matching conditions, particularly those at the second gate.

Self-Aligned Ion-Implanted T-Gate Technology for High-Speed GaAs Logic*

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The fastest room temperature logic gate operation yet reported has recently been achieved with an improved technology for self-aligned ion-implanted GaAs MESFETs. Overhanging 0.75/0.6 μm "T-gate" structures fabricated using metal lift-off and reactive-ion etching serve as a self-aligned mask for a high dose Si ion implant, thereby forming n^+ source and drain regions extending to the gate edges. This technique with only 3 lithographic steps (presently done by electron-beam lithography) offers the advantages of high yield and uniformity in a completely planar process that requires no wet chemical etching for device isolation or gate recess.

Normally-off FETs, DCFL inverters and 5-stage ring oscillators of various gate lengths were fabricated by direct implantation into LEC GaAs. The best high-speed operation has been obtained with ring oscillators using driver FETs with 0.6 μm-long, 11.5 μm-wide gates and linear resistor loads. At a bias voltage of V_{DD} = 3.7 V, these circuits exhibited minimum propagation delays as low as 15.4 ps/stage with a power dissipation of 5.4 mW/stage and power-delay product of 83 fJ. A 100% RF yield was obtained, with all 12 of the ring oscillators of this type on the wafer being fully operational, and none having a minimum propagation delay longer than 17.0 ps. At V_{DD} = 1.5 V, the oscillators exhibited propagation delays of 21.8 - 23.0 ps at power-delay products of 17 - 18 fJ.

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Effects of Cooling on a GaAs MESFET's Logic Circuit - Computed and Experimental Results

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Introduction

It is well established that the basic performances of a FET, mainly the transconductance and noise parameters can be improved by cooling. Our aim in this work is to demonstrate the same improvement for logic circuits. First we have observed an important effect of cooling on the maximum clock frequency of a MESFET's GaAs integrated circuit. In this paper we further study this effect by comparing experimental and computer results on a ring oscillator especially designed in our lab.

Experiment

A ring oscillator has been chosen as a test vehicle in this experiment. It consists of three simple inverters, and has been implemented in a hybrid circuit using discrete GaAs MESFET's (Plessey GAT2). The basic inverter is made up of two transistors - a driver and an active load. The necessary level shifting for logic compatibility is accomplished by capacitive coupling between successive inverters;and each input gate is biased in the midst of the logic swing.

Modelling

We used the model, based on a two-piece linear approximation of the velocity-field characteristic, which has been proposed by Grebene and Ghandhi. This model relies on 9 parameters which have been measured at different temperatures from ambient to 77K.

An original computational method, which takes into account the nonlinear behaviour of the FET, has been developed.Waveforms at each point of the circuit are constructed step by step, and at each step the new values of voltages, currents and capacitances are computed.In order to compare experimental and computed results, parasitics must be accounted for : case capacitances are measured and wiring capacitances are evaluated and fitted to obtain a good agreement at 300°K.

Results

We measured an increase of the oscillation frequency from ambient to liquid nitrogen temperature : 450MHz to 750MHz; but the power delay product remains nearly constant, results which are in good agreement with the simulation.

Measurements on individual devices have permitted the establishment of the dependence of the model parameters with temperature.We especially noticed an increase of the mobility which seems to be the main factor in speed improvement.

Conclusions

We have shown the interest of cooling, for logic circuits using GaAs MESFET's (mainly an improvement of speed in our case) and the availability of our simulation. As a conclusion we will discuss on the main limitations of our experiment (choice of a hybrid structure for the ring oscillator and choice of a classical two-micron-gate FET), and from these limitations we will introduce the next part of this work which is the design and the realization of a FET, and of an integrated circuit well matched for 77K operation.

Electron-Beam Fabricated Sub-Micron Gate GaAs FET's for Microwave and Logic Circuits

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Deep recessed gate MESFET's have been processed using direct-write electron beam lithography in lengths ranging from .4 microns to 1 micron. A short electrical source to drain spacing of .7 micron for a .5 micron gate length results from the deep recess. This recessed gate structure yields high transconductance g_m, low noise figure and low "on" resistance.

A .5 micron long by 300 microns wide low noise microwave FET was fabricated on a MBE grown layer which exhibited a transconductance of 160 mS/mm, a knee voltage of .75 V, and an output resistance of 83 ohm-mm. At 11 GHz, a minimum noise figure of 1.8 dB was obtained with an associated gain of 8 dB.

Direct-coupled FET logic inverters, NAND gates and five stage ring oscillators with normally-off driver stages and saturated resistor loads were fabricated on LPE material. A transconductance of 180 mS/mm at V_g = .8 V was achieved with an "on" resistance of 5.7 ohm-mm. Propagation delays as low as 26.64 psec per stage have been measured at a power dissipation of 3.62 mW/gate. The driver FET's were 1 micron long and 28 microns wide with saturated resistor loads 2 microns long and 3 microns wide.

Fabrication technology will be discussed also.

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Computer Modelling of a Dual Gate MESFET Mixer

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A recent forecast has suggested that the Direct Broadcast Satellite (DBS) television receiver will have a market potential of up to nine million sets per year, worldwide in about four years time. Each unit will require an outdoor 0.75m dish and down converter able to operate under rigorous conditions of temperature and vibration. At the heart of the down converter is a microwave mixer and for this application the dual gate GaAs FET device has shown itself to have a number of advantages. Chief among these is that it has a conversion gain, with 14dB at X band already reported. The signal and local oscillator inputs are fed separately to the two gates thus eliminating any complicated coupling and the device is particularly suitable to form the basis of a MMIC front end.

This paper will describe work in progress to develop an equivalent circuit mode of the dual gate FET used as a microwave mixer in a form which can be related to material properties and device performance. This is a large signal model including high frequency transit time effects which takes as its input the I_{DS} ~ V_{DS} characteristics of a FET, either from measurements or calculated as a result of the simulation work carried out at Leeds. The improvements in design suggested by the model in terms of material parameters and circuit conditions will be presented.

Two-Dimensional Simulation of Submicronic Space Charge Modulated F.E.T. Structures

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In small size devices, electron transport is mainly governed by non steady-state conditions for which new physical phenomena may occur and classical theories fail. Monte Carlo particle simulation, taking automatically the transient properties of electron dynamics into account, consequently is a very powerful tool for studying submicron devices. As devices are getting smaller, two-dimensional effects become more and more important. Accordingly we have developed a two-dimensional Monte Carlo simulation of electron transport in order to study new type of submicronic F.E.T. structures with an undoped active region. These structures are of interest especially for two reasons :

- (i) In such structures, carriers are moving in a nearly intrinsic region, thus ionized impurity scattering does not occur and, due to non stationary conditions, very high drift velocity values can be achieved.
- (ii) A very low gate voltage is only required to modulate the space charge region and control the source to drain current.

The specific features of electron transport in these types of F.E.T. structures are studied for various conditions such as, various active region length, gate length or gate location etc.... and it is shown that electron drift velocity along the F.E.T. channel can exhibit very high values. The I.V. characteristics are determined and compared to corresponding experimental values. Moreover, the F.E.T. parameters are deduced and it is shown that very high transconductance values can be achieved and cut-off frequency as high as a few hundred Giga Hertz can be expected.

A Computer Simulation of Small Signal Compression on GaAs FET Limiting Amplifier

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When an amplifier is driven into saturation it shows the same noise and small signal suppression phenomena as found in passive limiters : that is, with two signals (one could be white noise) at the input of a passive or active limiter and at least one passing the limiting threshold, the output power difference is bigger than the one at the input.

Based on the GaAs FET common source DC characteristics, the drain current is obtained as a function of gate voltage (input signal) bias and load line. The output voltage is this current multiplied by the load and could be approximated by a quadratic function. Finally the fast Fourier transform is used to find the output power spectrum. The computer program has been developed on an HP 984S minicomputer.

With just one signal at the input the simulation is useful to compute harmonics at different bias and different load line. With two signals at the input and at least one driving the GaAs FET amplifier into saturation, the program will output small signal suppression as a function of bias, of relative level of the two signals and of load line. When a GaAs FET is saturated with an increasing input signal the gate to source voltage becomes positive, the drain current initially increases, then decreases and finally saturates again to a value close to the IDSS.

The simulation shows that small signal suppression is strongly dependent on this portion of the DC characteristics and therefore on the right choice of the active device.

A Physical Model for the Large-Signal Characterization of Microwave MESFET Operation

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An accurate two-dimensional numerical analysis, based on a physical model, is used in the large-signal characterization of highly doped MESFETs. Thermionic-emission-diffusion boundary conditions are used to simulate the Schottky barrier gate and provide an improved model compared with the more commonly used diffusion approximation. A specially formulated current-continuity scheme allows GaAs devices with very high doping levels ($>10^{23}cm^{-2}$) to be characterized. A novel double iteration technique is used to increase the speed of the simulation, allowing long simulation times (>250pS). Simulated static I_{DS}-V_{DS} characteristics of short gate length MESFETs match measured data very closely.

The highly efficient physical model allows the steady state large-signal r.f. responses (c.w.) of microwave circuits to be accurately evaluated. The device is embedded in a time domain circuit model from which the terminal current and voltage responses are extracted. A lumped element circuit model is particularly appropriate for the characterization of microwave monolithic circuits. A careful formulation of the numerical circuit algorithms ensures accuracy and stability. By modelling the circuit as a one-port and Fourier analysing the terminal responses, the equivalent device admittance can be represented as a device surface over a range of frequencies and signal amplitudes. This approach has been successfully applied to the analysis and optimum design of microwave MESFET oscillators.

Comparative Survey of Several Models for Submicrometer Gate FET's

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Submicrometer gate FET constitutes a basic element in analogue and digital hybrid or integrated circuits. In order to predict the expected performances, and to optimize the device, a precise model is needed; for this purpose, it must take into account the non stationary electron dynamic effects.

In the past, we have developed a desk computer model based on the unidimensional assumption and the use of energy and momentum relaxation equations. For low noise or power usual devices (planar or recess structures), it gives very quickly accurate predictions of microwave performances (gain bandwidth product, noise figure, breakdown voltages). Its application field was recently extended with success to dynamic behaviour under large signal operation and several first results are given.

Monte Carlo simulation constitutes a more exact model; it is needed mainly for new structures such as space charge injection FET's, in which two dimensional effects take a particular importance. But unfortunately, it is not accurate taking into account the random nature of carriers motion (noise diffusion). Consequently, transient and dynamic regimes cannot be studied with a sufficient accuracy with realistic computer times.

Recently, we have developed an alternate model that will be described in the paper; it is based on the two dimensional resolution of Poisson, continuity and energy relaxation equations. It can be used for various structures and gives a precise description of physical device behaviour and an accurate prediction of performances. Several first results are given and its capability to describe transient and dynamic regimes is discussed.

GaAs Heterojunction Bipolar Transistors for Microwave Applications

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A review will be given of recent progress on GaAs Heterojunction Bipolar Transistors (HBT's) for microwave operation. A significant enhancement of the electron velocity has been demonstrated in GaAlAs-GaAs HBT's with abrupt emitter base interface and a thin base region. The design, fabrication and HF performances of the device will be presented. Recent results include improved growth of epitaxial layers by molecular beam epitaxy on semi insulating substrate, control of current gain by graded interface, and hot electron effects. Some key parameters such as base resistance, current gain-bandwidth product, output power will be discussed.

Design and Fabrication of GaAlAs/GaAs Bipolar Transistors : Application to Power Microwave Devices

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This paper is divided up into three parts. The first one is a brief survey of the capabilities of the heterojunction transistor and presents an original method that allows the design of an optimized HF power device. The second part describes the features of the devices that have been fabricated by liquid phase epitaxy. The third one shows up the relationship between the technological properties and the electrical behaviour on the basis of experimental results obtained on a number of structures; in particular the HF power amplification performances on the devices are reported.

The realization of a wide gap emitter brings about an additional degree of freedom for choosing the doping profiles of the heterotransistor. For this reason and also because of the high mobility values for the electrons in GaAs the obtained devices show a significant increase of both the output dynamic range and the frequency behaviour if compared to the silicon counterparts of the same geometry. As a consequence the use of the heterojunction transistors in the area of power HF signals is of great interest. A computation method is presented that trades-off the electrical parameters of the transistor and that allows determination of the base and collector characteristics. Such a possibility is illustrated by showing a full design project of the device.

Our mesa type samples were processed by liquid phase epitaxy. The doping profile and other geometrical characteristics of the various regions fulfil the requirements deduced from the previous theoretical study. The p-GaAs base layer is 0.2 - 0.5μm thick and is strongly doped ($N_A \simeq 10^{19}cm^{-3}$), the n-$Ga_{1-x}Al_xAs$ emitter with an aluminium rate $x \simeq 0.4$ is weakly doped $N_D \simeq 10^{17}cm^{-3}$.

The trends of both the current gain and the transition frequency characteristics can be accounted for on the basis of the technological data. The extreme features for the device's behaviour as obtained on several samples are the following : $h_{FEMAX} \simeq 3000$, $f_{TMAX} \simeq 3GHz$, $BV_{CBO} \simeq 120V$ $I_{CMAX} \simeq 10A$.

Bipolar Heterojunction Transistors for High Performance Linear and Ultra High Speed Digital Circuits - An Investigation of the Potential

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An investigation has begun into the theoretical requirements and practical limitations of bipolar heterojunction integrated circuits for high performance linear and ultra high speed digital applications.

Recent publications [1,2,3] have emphasized the high bandwidth product, f_T, attainable with the heterojunction technique in conjunction with highly doped very narrow base widths ($\sim$ 0.1 μm). Little discussion is presented on the optimum compromise for the base doping profile for both f_T and base resistance.

In the first stage of this investigation, first order theory of the device and experimental results have been correlated to indicate the most cost-effective route to a device with real applications. Specifically, experimental results will be presented itemising current vs. voltage relationships, current gains, gain bandwidth products, base resistances and junction capacitances for GaAlAs transistors with different base doping profiles. Epitaxial layers have been grown using both liquid phase epitaxy and MOCVD techniques and transistors defined by selective etching, contact definition and metalisation.

Early consideration of all the characteristics of the bipolar heterojunction transistor in conjunction with circuit design requirements will direct device optimisation to maximise the range of application of this technology.

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Edge Crowding Phenomenon Analysis in GaAlAs-GaAs Heterojunction Bipolar Microwave Transistors

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GaAlAs-GaAs heterojunction bipolar transistors are receiving increasing interest for high-frequency operation. In particular, they would offer, compared to silicon transistors, more attractive power performance due to the low base resistance. Indeed, this advantage would minimise emitter current edge crowding which is the fundamental limiting phenomenon for microwave power transistors.

This phenomenon has been well studied for D.C. operating conditions but, to our knowledge, no study has been attempted for dynamic large-signal conditions.

In order to clarify this question we have performed a numerical simulation based on equations describing current and voltage evolutions at the emitter-base junction as a function of the time and the location under the emitter finger. In this model all the displacement currents have been taken into account and the conduction collector current has been assumed to be induced and calculated by using the Ramo - Shockley Theorem.

Our analysis shows that, under class C operation, the currents and voltage behaviours are very different from D.C. predictions because of the importance of the displacement currents.

This analysis is used to predict the output power limitations and to provide an approach of the various design parameters, particularly the emitter width finger, in order to optimize power performances at a given frequency.

The Performance of GaAs MMIC Lumped Element Phase Shifters at S and C Band

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At S- and C-band frequencies, phase shifters using switched-line or similar distributed techniques become impractically large for realisation in GaAs MMIC form. For this reason, lumped-element phase shifters have been considered, the high-pass low-pass type being particularly suitable(1).

The performance of lumped-element networks such as these, is critically dependent both on being able to realise prime element values accurately on-chip, and in making due allowances during the design stage for the effects of parasitic elements. As such, phase shifters of this type represent a considerable challenge to the designer.

Initial work in this laboratory has concentrated on the design and fabrication of 90^{o} (±45^{o}) networks. These are particularly useful : they can form the basis for a complete 0-360^{o} phase shifter (1) , and are also necessary as 'building blocks' in other circuits, such as lumped-element quadrature hybrids and balanced mixers. The circuits which will be described in this paper are (a) a phase shifter covering the 2.5-3.5GHz band for use in phased-array radar transmitters and (b) a phase shifter for 5.8-7.2GHz used in the front-end of a monolithic 6-4GHz receiver (2) .

The authors would like to thank their colleague J.P. Suffolk for many useful discussions during the development of these MMICs. Part of this work has been carried out with the support of Procurement Executive, Ministry of Defence, sponsored by DCVD. The work described in this paper has also been performed in part under the sponsorship and technical direction of the International Telecommunications Satellite Organisation (INTELSAT). Any views expressed are not necessarily those of INTELSAT.

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A Two-Stage, Modular Cell Monolithic Power Amplifier

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A GaAs MMIC X-band two stage amplifier has been built based on a modular cell design principle. It consists of three separate identical cells. Each cell has one input and two outputs. The first stage has one single cell while the second stage has two, so that the power level per cell remains approximately the same.

The input cell is a double drain FET with identical matching circuits at each port, feeding the input of the second stage cells. The matching circuit consists of a shunt loop inductor, a transmission line and a series overlay capacity. All stages utilise FET transistors with four 100 μm wide, 1.3 μm long parallel connected gates.

The amplified signals of the last stage are combined together at the output in a conventional passive way. All the transistors are biased to the same drain and same gate voltages. The output power levels of each cell are very similar so that crosstalk on the chip is relatively unimportant. The design avoids low impedance matching problems and spurious phase shifts as in the case of large power transistors.

A 7 dB gain amplifier operating between 8 and 9 GHz was made to demonstrate its advantages.

The Noise Figure of the Microwave Distributed Amplifier Using FETs

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This paper calculates the noise figure of the distributed amplifier and shows that there is an optimum phase change per section which minimises the noise figure. Furthermore this calculation shows that the noise figure decreases as the number of stages is increased and that there is an optimum combination of number of stages and gate line impedance to minimise the noise figure.

This minimum noise figure is almost identical to that obtained from an optimally matched resonant FET amplifier without the consequent mismatch and bandwidth constraints.

MIM Capacitor *Dielectrics for GaAs MMIC's*

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The need for a dramatic reduction in the space occupied by capacitative elements of GaAs microwave monolithic integrated circuits (MMIC) has led us to study some of the possible dielectric films compatible with monolithic i.c. fabrication technology. Using the same set of electrode geometries, realised on semi-insulating GaAs substrates, we have compared a wide range of parameters obtained with films of silicon dioxide, silicon nitride, Al_2O_3 and Ta_2O_5 as deposited by triode sputtering. The films have been analysed physically in terms of their homogeneity, surface aspect, and particularly the reproducibility of thickness deposited. Electrical measurements include determination of capacitance from 100Hz to 10MHz, and 2-18GHz from which the variations of dielectric constant (ε) with frequency are determined. In addition, variations of leakage current and breakdown voltage are compared for different sample geometries, in particular the surface/edge ratio of the capacitor and the structure of, for example, dielectric coverage of *metallisation steps. It is notable that, especially* for the electrical measurements, the behaviour of the "semi-insulating" substrate can influence considerably the apparent properties of a MIM capacitor. A limited number of chemical measurements (Auger profiling, Rutherford Backscattering Spectroscopy) have also been undertaken. We will report various results of the above study which lead us to conclude that Ta_2O_5 is a promising alternative for capacitors in high density MMIC's currently being realised in our laboratories

A Broadband Planar GaAs Amplifier/Oscillator for Monolithic Micro- and Millimeter Wave IC's

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The purpose of this paper is to report new experimental results obtained with a novel device structure recently developed at our laboratory (1)(2). This device is a planar transferred electron device with a MESFET-like cathode contact providing limited constant electron injection into a fairly long drift region. The basic underlying principle is that the usual transit-time oscillations ("Gunn oscillations") are suppressed by applying a sufficiently large negative bias voltage to the gate leading to a stable stationary depletion layer or uniform field distribution in the drift region (3). As a consequence of this the device exhibits a frequency-independent negative differential terminal resistance and can thus be made much longer than the transit-time principle would require. The frequency of operation is determined solely by the load impedance and no more by the length of the drift region. The gate electrode is shorted ac-wise by a thin quartz layer placed between source and the overlapping gate which minimizes losses caused by the low field region between gate and source.

Experimental Results

Experimental results obtained with devices having 10, 20 and 28μm long drift regions confirm that stable amplification and power generation at non-transit-time related frequencies above the transit-time frequency is attainable without special bias and tuning circuit adjustments (2)(3). In all these experiments the frequency of operation was determined solely by the load impedance except for gate bias levels between -2V and 0V, at which transit time oscillations occurred as is expected for TED's with overcritical NxL product ($10^{13}cm^{-3}$).

In this paper further results obtained with devices mounted in both stripline circuits (8-16GHz) and in Ka-band waveguide circuits (26-40GHz) will be presented and discussed in detail.

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(3) G. Rieder, H. Thim, R. Kuch and K. Lubke, to be published AEU.

1.12 Gb/s Multiplexer IC on GaAs for Laser Modulation

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The paper describes an arrangement for laser modulation at 1.12 Gb/s. It consists of a GaAs MESFET-IC with multiplexer function and a separate clock generator. The GaAs IC converts four 280 Mb/s signals into a 1.12 Gb/s RZ signal at the output. Especially at high modulation rates, the RZ format is mandatory in respect to suppression of pattern effects of the laser and the speckle noise.

The IC contains 4 Schottky diode AND gates, followed by a Schottky diode OR gate with 4 inputs. The multiplexed signal at the OR gate output is fed via MESFET source follower to the driver stage which is realised as a 4 gate finger MESFET. MESFETs and Schottky diodes are of the recessed gate type; the active layer is Se-implanted.

The clock source consists of a 280 MHz sinewave generator, a Si step recovery diode and 50 Ω-connecting lines with different lengths for the necessary delays.

This type of modulation circuit allows relatively fast laser control with only a few components and a simple IC. Timing problems, which may arise in high scaled integrated circuits can be solved easily in this concept by adjusting the lengths of connecting lines. In addition the simple GaAs IC guarantees a high fabrication yield.

GaAs Clocked Comparator Operating at 1.8GHz

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A new ultra high speed GaAs strobed comparator has been designed and extensively characterized.

This comparator is designed to be a building block for a very fast parallel analog to digital converter (ADC).

It is well known that in ADCs, the conversion speed, the accuracy, and the resolution are all strongly affected by the comparator performances. Then, in order to get a very high gain with the fastest time response, we have used a dynamic amplifier consisting of a flip-flop regenerator. Our comparators use basically two BFL multiplexing gates and - depending on the clock state - they are used either as amplifier or as latch.

The circuit has been fabricated using the self-aligned technique with minimum under-etching. The switching FETs has a gatewidth of 15μm and the pinch-off voltage is -1.2V. With these characteristics, the comparator shows good operation at a clock frequency up to 1.8GHz. The resolution is better than 50mV. The power consumption is 45mW. The offset voltage has been measured over the wafer and had a mean value of 10mV with a standard deviation of 40mV.

This experimental comparator demonstrates that good performances can be obtained using regeneration. This comparator should be useful for very high speed ADC at Gigabit sampling rate.

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$Ga_{0.47}In_{0.53}As$ FETs and Related Problems

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Besides the application of the quaternary GaInAsP-system for electro-optical devices this material is well suited for microwave applications too. Especially GaInAs lattice matched to InP allows the fabrication of bipolar and field effect transistors.

The paper will give relevant material data and show the feasibility of MISFETs and JFETs.

Because Schottky contacts are difficult to realize for JFETs pn junctions have to be used which can be fabricated by ion implantation or diffusion. Also hetero structures can be applied. Regarding the MISFETs the better electronic properties of GaInAs in respect to InP counterbalance the inferior interface behaviour.

Results on contact resistance which also favour the narrow gap material and detailed data on Be- and Cd-implanted layers will also be given.

High Velocity Electrons for Compound Semiconductor Transistors

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The ballistic limits for electron velocity with gradual acceleration across an active region of a device is just over 4 x 10^7cm/s and can be obtained when short horizontal or vertical FET devices have reduced ion density and are less than .5 micron thick. The ballistic injection of about .25 eV electrons into a region of about 2,500 V/cm electric field allows an average drift velocity of just over 8 x 10^7cm/s for about .75 micron. Either a planar doped barrier or a heterojunction potential drop can be used to launch the ballistic electrons in the latter case. The use of Schottky gate control for electron injection and drift can be made. Ballistic electrons lose momentum at a substantial rate when passing through n-type regions with thermal electron densitites of 5-10 x 10^{17}/cm^3, due to plasmon launching. This effect is substantially reduced in p-type material, although electron-hole scattering occurs. The use of these ballistic electrons in FET and heterojunction bipolar devices will be explained, and the expected frequency response beyond 100 GHz will be presented. Some comparison with theoretical and experimental efforts at other laboratories will also be made.

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The Properties and Performance of Monolithic Hot Electron Transistors

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The monolithic Hot Electron Transistor offers the potential of gain at frequencies well above those where a bipolar device can no longer operate. This arises because of the unipolar nature of hot electron transport up to high current densities combined with minimal junction capacitance and charging time. Furthermore, being unipolar with a mutual conduc.ance proportional to emitter current the device combines some of the best features of F.E.T. and bipolar action.

This talk will outline the basic concepts involved. Hot electrons are injected over a bulk unipolar barrier and move by diffusion across a narrow degenerate base region before overcoming a second bulk unipolar barrier which acts as a collector. There is a contribution from ballistic electrons but this is usually small. Assuming a useful transport factor, the performance of devices in silicon and GaAs will be compared.

Experimental results on devices formed in silicon will be discussed together with some of the technological difficulties.

InP/InGaAsP Bipolar Transistors for Optical Receivers

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Heterojunction bipolar transistors (hbts) based on the material system InP/InGaAsP evolve as the most promising structures for integrated photo-receivers in optical communication systems at 1.3 to 1.5μm wavelength. We will report on our design and technology of such transistors mostly realized as fast phototransistors with a base connection(1). The advantages of a base connection in these phototransistors compared to reported designs without(2) are : low noise, higher collector breakdown voltages (no open base!) and high-speed mode operation possible. The applied technology is easily extendable to ICs.

Recently we achieved the necessary extension of the wavelength range to 1.5μm by using a liquid phase epitaxial growth sequence of n^--InGaAsP (λ_c = 1.56μm) as the collector layer, p^+-InGaAsP (λ_c = 1.3μm) as the base layer and n-InP as the emitter layer. By this we suppressed the dissolution tendency while growing the widegap InP emitter on top of the small-gap InGaAsP.

Base contacting by selective etching and by p^+-diffusion are compared. While the diffusion process further degrades the base-collector doping profile, it allows smaller emitter structures and has advantages for low current devices due to lower base recombination losses. The interdevice isolation of these hbts can only be made by mesa etching; proton implantation as in case of GaAs/GaAlAs fails. This will seriously hamper large scale integration but can be tolerated for small scale integrated photo-receivers.

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High Power InP MISFETs

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InP is well suited for power FET's because of its high peak velocity, low ionisation coefficients and good thermal conductivity. Because of the low Schottky barrier, InP MESFETs have a high gate leakage current which prevents high voltage operation. The use of MISFET's with SiO_2 insulated gate suppresses the gate leakage current and therefore considerably reduces the ionisation in the channel.

We have made depletion MISFETs on 0.5µm thick, 1.2 x 10^{17}N type epitaxial layers. The channel is recessed to a thickness of 0.2µm, and a 100 nm pyrolytical SiO_2 is deposited at 380°C. The GeAuNi contacts are distance 4.5µm and the Al gate is 1.5µm long and 300µm wide.

Typical values of I_{DSS}, transconductance and pinch-off voltage are : 200 mA, 20 mS, 18V.

The performances of the best device at 9 GHz are :

- Small signal gain 7 dB at V_{DS} = 6V
- Output power at 4 dB gain : 920 mW, or 3.07 W/mm of gate width, with a power added efficiency of 36%. The bias conditions are V_{DS} = 13.5V, I_D = 114 mA.

This power output per unit gate width is more than twice the best performance obtained with GaAs power FET's. This is mainly due to the high value of I_{DSS} per unit gate width, and to the high surface potential excursion that can be induced through the gate insulator at high frequencies.

The Pulsed Behaviour of Quasi Normally-Off GaAs MISFET's

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A common feature of slow d.c. sweep MIS measurements on GaAs surfaces is surface potential pinning arising from filling of the surface states. The pulsed field-effect has been employed using IGFET structures to test whether electron accumulation could be achieved on n and p GaAs surfaces under pulsed conditions. These effects were not observed in times as short as 30ns suggesting that charge enters the pinning surface states in much shorter times. The structures which were tested employed plasma oxidised alumina as the gate insulator.

The operation of an n-channel GaAs IGFET in a quasi-normally off mode has been demonstrated. The maximum off-state time was about 1s at room temperature and was determined by the emptying of the pinning surface states by hole capture. The rate limiting process has been shown to be the supply of holes by thermal generation.

The main advantages of this device are :

(i) the possibility of directly coupling logic gates

(ii) simplicity of manufacture

(iii) larger noise margin and less stringent voltage tolerances than are required in enhancement-mode MESFET approaches

(iv) the exploitation of surface states which have well defined energies at the insulator/n-GaAs interface.

The predicted speed and speed-power products are comparable with those for other GaAs enhancement mode structures.

Improved Noise Performance of Millimetre Wave Silicon Impatts

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Over the years Impatt devices have built up a reputation for being noisy devices. At the lower microwave frequencies this assumption is well founded, resulting in the choice of Gunn diodes for low noise local oscillator applications. At millimetre wave frequencies, however, the situation is quite different, since the rapidly decreasing efficiencies of the Gunn device lead to low output powers. Through careful control of material quality, processing techniques and circuit design, we have produced double drift silicon devices exhibiting low noise behaviour with power outputs up to 200-300mW (6-10% efficiency). Their f.m. noise performance, in terms of noise to carrier ratio, is comparable to that of Gunn devices far from carrier, and considerably better closer to carrier (<1MHz offset). Measurements at 40GHz and 80GHz have shown that the noise measure of these devices remains constant (at ∿33dB) up to 75% of full output power, which is the most suitable operating point for high reliability. Above this value the noise increases rapidly as high junction temperatures are approached. Measurements of the noise to carrier ratio exhibit a white (constant deviation) spectrum at offset frequencies greater than 1kHz offset.

It is possible to explain this improvement in the noise performance of silicon Impatts at mm wave frequencies on the basis of theoretical models of the device behaviour.

Our results suggest that the Impatt can provide a viable alternative to Gunn devices for local oscillator applications, particularly for systems where many mixers are involved.

On the Efficiency of Pulsed and CW Impatt Diodes

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The design of pulsed Impatt diodes is less well understood than their CW counterparts due to the non-constant junction temperature and the very high current density used. This paper will present a simple analytic design theory for these devices which is applicable to both pulsed and CW Impatts. It will be shown that the very high current density used for pulsed devices results in a reduction in efficiency and that a trade-off exists between peak pulse power and efficiency. It will also be shown that this effect is far more severe for Si flat profile devices than for GaAs pseudo-Read profile diodes. Experimental results of power and efficiency for various doping profiles will be presented and compared with theoretical predictions.

Fast Risetime GaAs Read Impatts

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The switch on characteristics and intraspectral line noise of free running, phase primed and phase locked pulsed GaAs Impatts have been measured. High power, high efficiency single drift 'Read' Hi-Lo profile devices have been studied in detail and comparison is made with double drift GaAs Impatts and InP TEOs.

In a pulsed oscillator the r.f. growth is determined by the relationship between the small signal and large signal negative resistance exhibited by the active device. The change in device impedance affects not only the r.f. risetime but also the magnitude and variance (jitter) of the r.f. pulse switch on delay with respect to the applied bias pulse. In addition a change in device susceptance between small and large signal operation determines the change in frequency between start up and stable operation.

Measurement of the intraspectral line noise of the pulsed oscillator gives information regarding the degree of pulse to pulse phase coherency(1). A measure of the noise associated with the spectrum may be obtained from the ratio of the power in the Fourier line - present under phase priming or phase locking - to that of the noise between lines. Evaluation of this ratio shows the InP TEO and the double drift uniformly doped Impatt to be greater influenced by the injected signal, due to their relatively slow r.f. growth rates, than the Read Impatt. This is confirmed by the values determined for r.f. risetime, delay and jitter being greater for the former devices than the Read Impatt, showing this device to be ideally suited to short pulse, fast risetime applications.

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Electronic Tuning of Trapatt Oscillators

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A novel technique for providing electronic tuning of a Trapatt oscillator is presented.

A varactor delay line is used to provide variable delay between the Trapatt diode and the filter in an Evans type oscillator arrangement. To demonstrate the feasibility of the technique an oscillator was built with a two stage delay line included. In order to tolerate the large voltage variations expected, each varactor stage was made up of two 90 Volt breakdown tuning diodes connected in series. Furthermore, the Trapatt diode was lightly biased to minimise the voltage variations propagating through the line.

With a centre frequency of 1.6 GHz, a tuning range of 20 MHz (limited by the tuning diodes breakdown voltage) with an output power of 8 watts ± 0.5 dB was observed. The results are in good agreement with theory.

Interface Formation of Metal on MBE-Grown GaAs (001)

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The initial growth of metals on MBE GaAs(001) has been studied by Auger electron spectroscopy (AES) and reflection high energy electron diffraction (RHEED). The submonolayer growth is characterized by a stage of dispersed metal atoms at the surface and is followed by metal nucleation. In addition surface processes such as interdiffusion[1] and chemical reaction occur depending on the initial surface reconstruction and temperature. An illustrating example is the growth of Al on GaAs(001). Above 500K the interface formation is dominated by AlAs-formation followed by epitaxial growth[2]. At lower temperatures these reactions become less pronounced and a surface reconstruction dependence is also found[2]. Although different growth is observed on differently reconstructed surfaces, the band bending of C(4x4) and (4x6)-surfaces with 0.2ML Al is identical as observed with ultra violet photo electron spectroscopy (UPS). Furthermore the same bandbending is present also on the surfaces before Al deposition[3]. This together with the good agreement between the Schottky barrier height deduced from these measurements and electrical measurements of the barrier height for thick films, indicates an Al-barrier formation governed by properties of the MBE GaAs[4].

Emphasizing the Al/GaAs-system, for which the most complete set of data exists, data on the Au/GaAs- and Sn/GaAs-systems will also be presented for comparison[5].

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